

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
Angelo VISCONTI
Serial No. 10/782,725
Filed: February 19, 2004



: Atty. Docket: 02-AG-210/EV
: Group Art Unit: 2186
: Confirmation No. 3423
:

For: METHOD OF PROGRAMMING A MULTI-LEVEL, ELECTRICALLY
PROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY

INFORMATION DISCLOSURE STATEMENT

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
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SIR:

The attached Form PTO-1449 provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that other art than that identified exists; nor that the information provided is prior art; nor that a search has been made.

This IDS is submitted under:

- ☒ 37 CFR 1.97(b) - No Fee.
☐ 37 CFR 1.97(c) - No Fee, with Certification.
☐ 37 CFR 1.97(c) - Fee.
☐ 37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge any required fees under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. 50-1556.

Respectfully submitted,

Date: 7/13/04

By: Jose Gutman
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service by first class mail in an envelope addressed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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Form PTO-1449

U.S. Dept. of Commerce
Patent & Trademark Office

Atty. Docket: 02-AG-210/EV

Serial No. 10/782,725

List of Documents

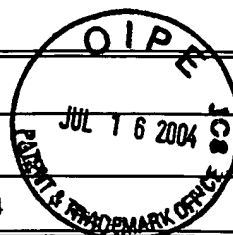
Cited by Applicant

(Use several sheets if necessary)

Applicant: Angelo VISCONTI

Filing Date: February 19, 2004

Group: 2186



U.S. PATENT DOCUMENTS

Ex'rs In'l		Document Number	Date	Name	Class	Sub- class	Filing Date, if applicable
	AA1	5,926,409	July 20, 1999	Engh et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Sub- class	Trans'l'n Yes/No
	AA2	EP 0 763 828	March 19, 1997	Europe			Yes
	AA3	EP 0 908 895	April 14, 1999	Europe			Yes
	AA4	WO 01/63613	August 30, 2001	PCT			Yes

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AA5	Roberto Versari et al., "Optimized Programming of Multilevel Flash Eeproms", ICECS 2001: 8 th IEEE International Conference on Electronics, Circuits and Systems, Vol. 2, September 2, 2001, pp. 945-948, XP010563149.
	AA6	David Esseni et al., "Trading-Off Programming Speed and Current Absorption in Flash Memories with the Ramped-Gate Programming Technique, IEEE Transactions on Electron Devices, Vol. 47, No. 4, April 2000, pp. 828-834, XP001131051.
	AA7	European Search Report dated July 25, 2003 for European Application No. 03425096.9.

Examiner:

Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.